

for IMS roaming. The P-CSCF, as the initial point-of-contact, may be in the home or a visited network. After just a few messages, the I-CSCF, having located the S-CSCF, bows out of the transaction. The S-CSCF does the heavy lifting for the call by determining the resources needed to handle a call successfully. If the call terminates at another UE in the same network, the S-CSCF locates a Packet Data Network Gateway (P-GW) to reach the targeted UE. If the call terminates at a UE in another service provider's network or at a landline in the PSTN, the S-CSCF locates the appropriate gateways to reach the requested destinations.

IMS is a converged architecture (figure 2) for wireless, wireline, and broadband. It is a layered architecture defining a Transport layer, a Control layer, and a Services Application layer for delivering voice and media traffic over IP.

The 3rd Generation Partnership Project (3GPP*) defines the details on the IMS architecture, functional elements, and interface requirements. As stated above, IMS is designed to support any access technology. The following link provides an overview of the 3GPP architecture, including a description

of all the network elements used in the IMS as well as those in legacy core networks:

3GPP TS 23.002 (<http://www.3gpp.org/DynaReport/23228.htm>)

This diagram shows both the control and media elements defined by 3GPP for IMS. In addition to SIP there are protocols specifically for Media transport: the real-time transport protocol (RTP) and the message session relay protocol (MSRP). The functions processing Media streams have stringent real-time requirements. Table 1 shows all the elements.

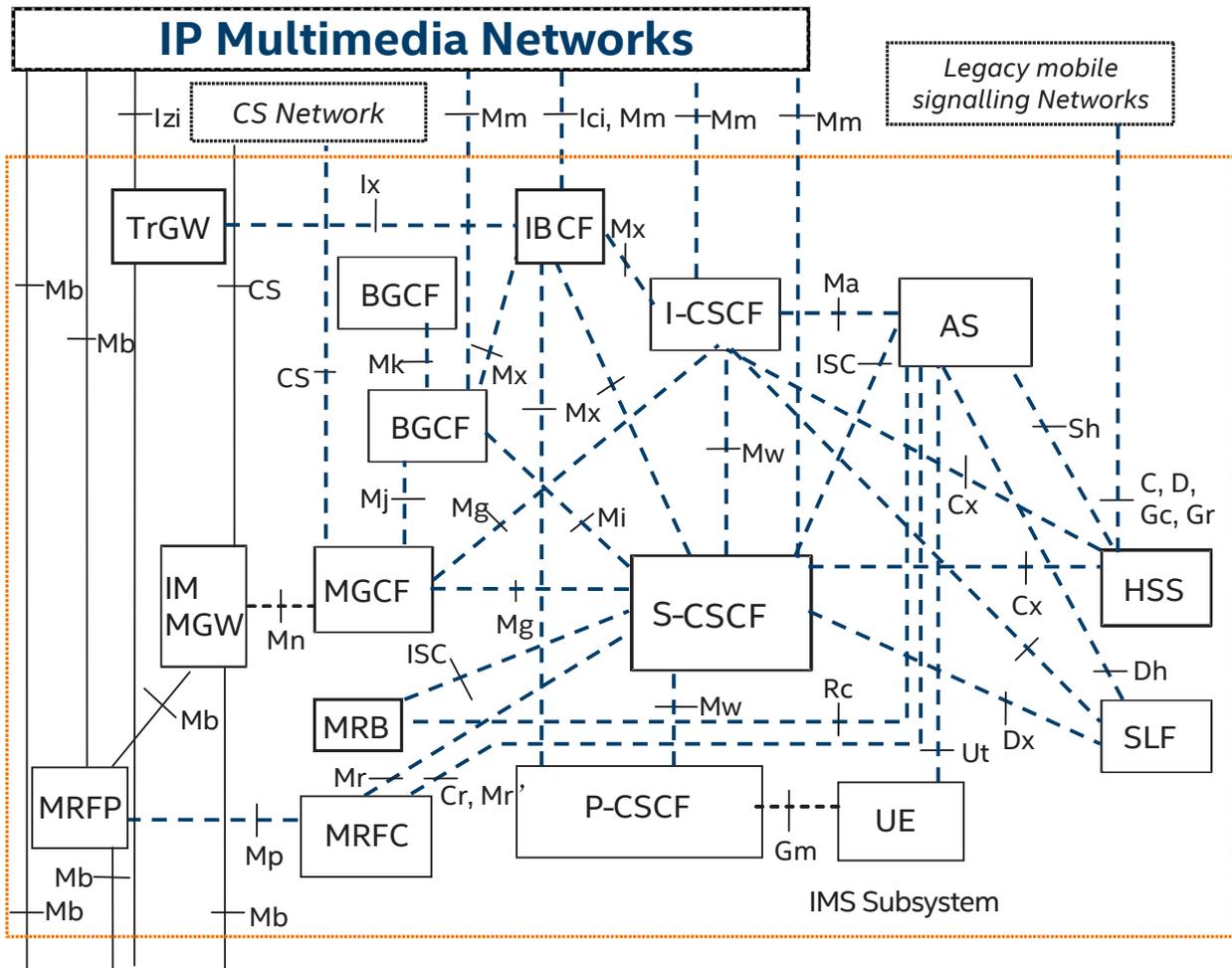


Figure 2. IMS reference architecture.

Table 1. IMS function examples.

IMS FUNCTION EXAMPLES	
P-CSCF	Proxy-Call Session Control Function
S-CSCF	Serving-Call Session Control Function
I-CSCF	Interrogating-Call Session Control Function
E-CSCF	Emergency Call Session Control Function
AS	Application Server
PS	Presence Server
IP-SM GW	IP Short Message Gateway
MMSC	Multimedia Message Service Center
VMS	Voice Mail Server
RCS	Rich Communication Services
MRFC	Media Resource Function Controller
AF	Application Functions (other)
BGCF	Breakout Gateway Control Function
MGCF	Media Gateway Control Function
ATCF	Access Transfer Control Function
EATF	Emergency Access Transfer Function
MGW	Media Gateway
ATGW	Access Transfer Gateway
WebRTC GW	RTC-Real Time Communication

Figure 3 shows a diagram of a practical example of an IMS architecture topology for IMS.

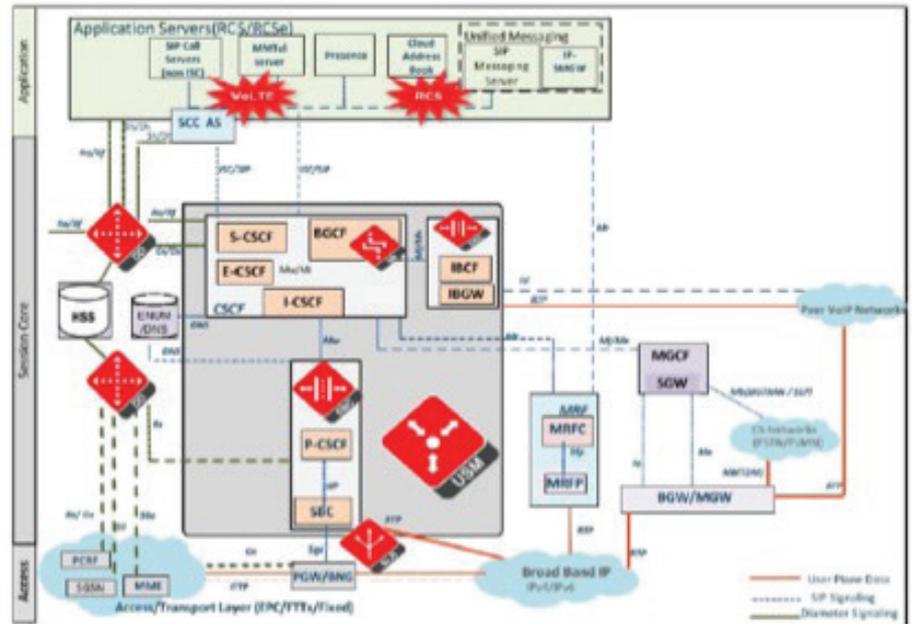


Figure 3. IMS network architecture topology (Oracle).

A practical approach for an IMS implementation is shown by Oracle to provide an integrated and fully 3GPP IMS-compliant CSCF core. Typically the P-CSCF is combined with interconnect functions to provide a Session Border Controller (SBC). Oracle have consolidated functional elements and minimized signaling interfaces, while providing all of the 3GPP IMS reference point interfaces needed to communicate with other external network elements.

Industry Solution Architecture: vIMS

The vIMS node can be logically divided into a control/signaling plane element and an element to process the Bearer traffic, also known as the data plane. The control/signaling plane element usually encompasses the CSCF and is possibly combined with the Telecom Application Server (TAS) function and runs today on standard common off-the-shelf (COTS) servers as a

virtualized network function (VNF). Initial deployments tend to consist of one large VNF; however, the industry is now taking a more modular approach.

Although not an IMS-defined element, the SBC has evolved to support a number of IMS-defined functions in part or in whole. Typically, on the access side of the network, the access SBC encompasses the Proxy CSCF and the Access Border Gateway Function (A-BGF). On the interconnect side of IMS is the Interconnect Border Control Function (I-BCF), which provides the interface to external networks. These components only handle the signalling element of the calls. An Interconnect SBC integrates the I-BCF with an Interconnect Border Gateway Function (I-BGF) element to allow the appropriate handling of the signalling and media traffic within a single system. While the Access SBC interfaces to all the user end-points, the Interconnect SBC interfaces to other networks over SIP trunks.

Figure 4 shows one possible solution implementation. The I-CSCF and S-CSCF have been combined with the Telephone Application Server as a VNF on an Intel® Xeon® processor. The Home Subscriber Server (HSS) is often seen as a mission-critical function, and while it exists on an Intel Xeon processor-based server, it is not virtualized. The SBC today often is implemented as a fixed function box. This will be described in more detail in the following section.

SBCs and Media Processing

The bulk of the traffic crossing a border is the media, which has been growing significantly. It's equally critical for the service providers to control the nature of the media traffic they admit into their network and to control the nature of the media traffic they pass on to a peer. Media processing encompasses media-handling functions, such as transcoding, conversion of a media stream from one codec type to another, dual-tone multi-frequency (DTMF) interworking functions, where DTMF tones within the media flow are detected and converted into RFC2833/RFC4733 format, or fax interworking, where G.711 fax is converted to T.38 fax.

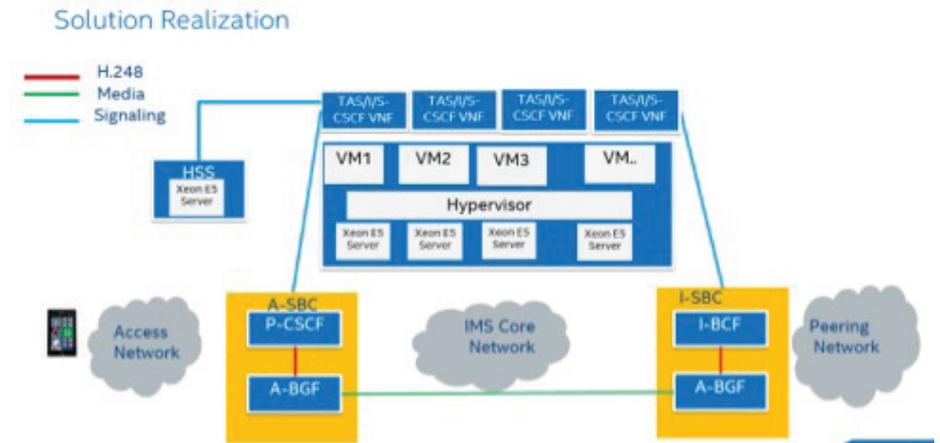


Figure 4. Solution implementation.

WebRTC IMS Considerations

A Web Real-Time Communications (WebRTC) client could communicate at the control plane with an inter-working function (IWF), the WebRTC IWF, via the GWeb reference point. (GWeb is the name of the interface between the WebRTC client and the WebRTC signaling function.) The WebRTC IWF communicates with the P-CSCF via

the Gm reference point, which is the reference point between a UE and a P-CSCF or between an IP-PBX and a P-CSCF.

The WebRTC IWF unit is typically owned by the IMS service provider but may be owned by a third party as well. A diagram of the WebRTC Client and interfaces to the IMS functions is shown in Figure 5.

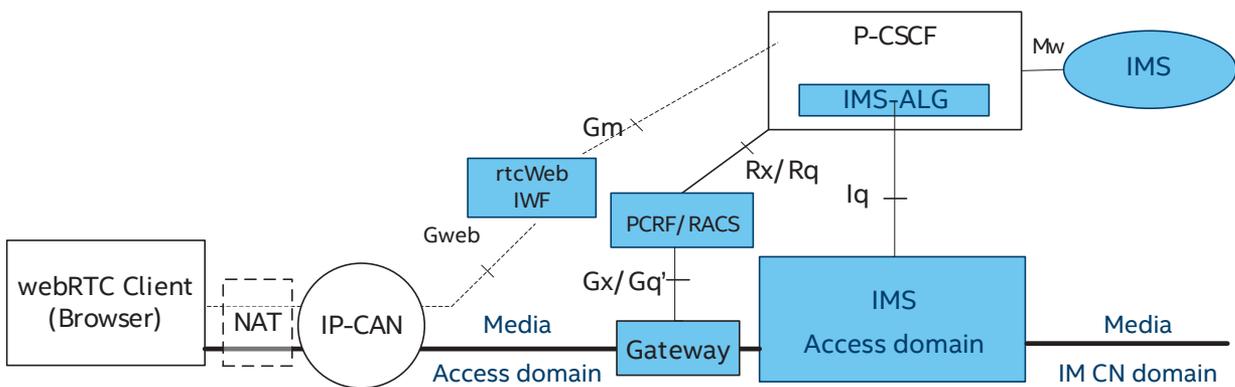


Figure 5. WebRTC architecture.

Rich Communication Services (RCS) IMS Considerations

A sample architecture to support RCS is shown in Figure 6.

The Packet Switched/Circuit Switched (PS/CS) gateway (GW) is used for interworking. The Message (MSG) Store element relates to the CPM (Converged IP Messaging) Store Server. Legacy MSG refers to the Short Message Service (SMS)/Multimedia Message Service (MMS) services that may be utilized via an IWF (Interworking Function) located in the group of Application Servers (AS), which, in addition to these IWF node(s), may also include various other nodes used by the RCS services, for example:

- Presence Server
- Messaging Server
- XML (Extensible Markup Language) Document Management (XDM) Server (XDMS)
- Multimedia Telephony (MMTEL) Application Server

The RCS specification at <http://www.gsma.com/network2020/specs-and-product-docs/> contains more details.

Platform Reference Architectures

Table 2 shows an example of a hardware bill of materials suitable for the vIMS reference architecture.

Additional technologies including Enhanced Platform Awareness (EPA),² Intel® Resource Director Technology,³ Intel® QuickAssist Technology⁴ (Intel® QAT), Intel® Trusted Execution Technology (Intel® TXT),⁵ and Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI),⁶ among others, are all relevant to the IMS reference architecture. Please note that not all processors support relevant technology.

For the latest Intel Open Network Platform (ONP) reference architectures, please refer to .01.org.⁷

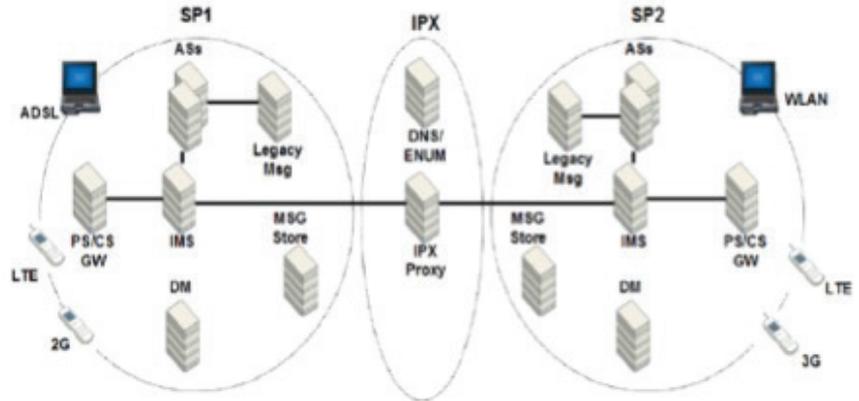


Figure 6. RCS architecture overview

Table 2. Example of a hardware bill of materials.

Processor	Dual Intel® Xeon® processor E5-2680 v3	
Platform	Intel® Server Board S2600WT 3 TB HDD Seagate Constellation* CS 2x Intel® Solid State Drive Data Center S3700 Series/200 GB	
Memory	256 GB Memory	
NICs	2x Intel® Ethernet Converged Network Adaptor X520-DA2	Niantic 2-port 10Gb. For the latest on controllers see Intel® Ethernet Controller
Add-In	Intel® QuickAssist Adapter 8950	PCIe* Gen 3 Refer to Drivers for Intel® QuickAssist Technology for the latest drivers and patches

Table 3. Links to specific capabilities.

Intel® Resource Director Technology	http://www.intel.com/content/www/us/en/architecture-and-technology/resource-director-technology.html
Intel® QuickAssist Technology	http://www.intel.com/content/dam/www/public/us/en/documents/white-papers/communications-quick-assist-paper.pdf https://01.org/packet-processing/intel®-quickassist-technology-drivers-and-patches
Intel® Trusted Execution Technology	http://www.intel.com/content/www/us/en/architecture-and-technology/trusted-execution-technology/malware-reduction-general-technology.html http://www.intel.com/content/www/us/en/architecture-and-technology/trusted-execution-technology/trusted-execution-technology-security-paper.html http://www.intel.com/content/dam/www/public/us/en/documents/guides/intel-txt-software-development-guide.pdf
Intel® Advanced Encryption Standards New Instructions	https://software.intel.com/en-us/articles/intel-advanced-encryption-standard-instructions-aes-ni http://www.intel.com/content/dam/www/public/us/en/documents/white-papers/aes-ipsec-performance-linux-paper.pdf
Enhanced Platform Awareness	https://software.intel.com/sites/default/files/managed/8e/63/OpenStack_Enhanced_Platform_Awareness.pdf https://networkbuilders.intel.com/docs/openStack_Kilo_wp_v2.pdf
Open vSwitch*	https://networkbuilders.intel.com/docs/open-vswitch-enables-sdn-and-nfv-transformation-paper.pdf
Data Plane Development Kit	http://www.intel.com/content/www/us/en/intelligent-systems/intel-technology/dpdk-packet-processing-ia-overview-presentation.html https://networkbuilders.intel.com/docs/aug_17/Future_Enhancements_to_DPDK_Framework.pdf
Hardware Offload	http://www.intel.com/content/www/us/en/ethernet-products/controllers/overview.html

vIMS Solutions Deployment Considerations

Performance

For all virtual applications, adequate performance on Intel® architecture-based standard high-volume servers (SHVS) is necessary to justify the business case to transition from physical- to virtual-based network functions. Therefore, the ability to run more virtualized applications on the same physical hardware enhances the business case for SHVS.

Intel's high CPU frequency, large caches, advanced pipelines, and hardware accelerators make them ideal for tasks such as large table lookups, hashing, parsing, and so on, which are required for the control/signaling layer processing. While voice/media transcoding on Intel CPUs is

possible, there are density challenges today and Digital Signal Processing (DSP) accelerators may be required. Important requirements for voice and media transcoding also include throughput, latency, and jitter.

To meet these requirements and to assure optimal utilization of data center resources, the environment should include the latest Intel® architecture-based chipset and the capabilities identified in the previous section (for example, pQoS, Intel QAT, Intel AES-NI, Intel TXT, EPA, and so on). This applies not only to the capabilities available in the infrastructure but also to the specific capabilities leveraged by the virtual applications.

Lab trials and proofs-of-concept (PoCs) continue to demonstrate and allow for the evaluation of different paths to reach optimal performance

for virtualized functions on SHVS. Standard kernel-based Open vSwitch* (OVS) has proved insufficient to meet the performance requirements to prove the business case for SHVS. While single root I/O virtualization (SR-IOV) enables better performance than standard OVS, it has certain dependencies (for example, hardware and specific drivers) that create an operational challenge. In addition, this architecture does not ultimately deliver the benefits of virtualization. However, results from recent PoCs and lab trials of Data Plane Development Kit (DPDK)-enabled OVS (user space OVS) have delivered performance results very near that of SR-IOV.

With this in mind, the recommended reference architecture to support the business case for the SHVS replacement of dedicated physical appliances must deliver an

environment that supports SR-IOV and DPDK-enabled OVS. This approach enables CSPs to get to market immediately on SHVS using DPDK-enabled OVS or SR-IOV, if required. The transition to DPDK-enabled OVS will support the realization of the benefits of virtualization, such as optimization and specific feature sets.

Operational

vIMS solutions also require the virtualization and integration of hooks across all layers of the software stack. As shown in the figure below, horizontal solutions must link capabilities across all the disparate layers of the NFV/SDN stack to actually deploy, monitor, and bill for services. Optimally, vIMS service realization requires an appropriate environment, with resource models coordinated with subscription plans and entitlements in the policy framework.

How, where, what, when, and how much?

There are important questions that must be addressed to effectively design, integrate, and operate any virtualized network solution (for example, how, where, what, when, and how much). The ability to deploy VNFs successfully on SHVS requires an understanding of the environment's capabilities and location that is well coordinated with the application's requirements. SHVS provides significant flexibility and workload placement from edge to core, driving the requirements for the operational tools to ensure the environment is trusted, secure, and has the appropriate resources for the task.

As an example, Intel is driving industry initiatives and making contributions, such as OpenStack⁸ EPA, to ensure

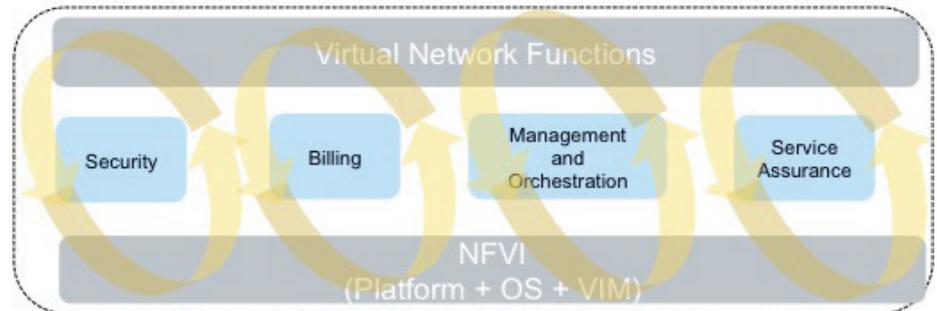


Figure 7. Horizontal solution linkage

that Intel architecture-based platform capabilities are exposed appropriately to the CSP's management and orchestration implementations and enable optimal data center resource utilization.

Network service life cycle management, monitoring, security, and billing models are all examples of the horizontal solution capabilities required to scale successfully in a virtualized environment. Intel is working closely with CSPs to enable and, in some instances, drive industry efforts to accelerate maturation of these horizontal capabilities. Future versions of this document will provide more detail and examples of those efforts.

As described in Intel's Service Provider Network Maturity Model,⁹ the initial deployments of network virtualized functions will rely on single-vendor implementations for end-to-end vertical solutions that include the necessary horizontal capabilities. As the horizontal capabilities mature and service providers transition from single-vendor implementations, the business case for creating commercial business services from the virtualization of network functions will continue to improve and will also help drive new revenue opportunities from the new offerings.

Next steps

- To learn more about Intel's technology for NFV, attend the courses available in the Intel Network Builders University at <https://networkbuilders.intel.com/university>.
- To learn more about Intel Network Builder partners for vIMS and other NFV products, visit <https://networkbuilders.intel.com/solutionscatalog>.
- To build a testbed using the Intel ONP Reference Architecture, download the documentation at <https://01.org/packet-processing/intel%C2%AE-onp>.
- To get the best security in your NFV systems, specify Intel Cloud Integrity Technology in your infrastructure and VNF procurements.
- To get the highest performance from your NFV systems, specify compatibility with the Data Plane Development Kit in your Infrastructure and VNF procurements.
- To get the highest return on investment from your NFV systems, specify use of Enhanced Platform Awareness in your Orchestration, Infrastructure and VNF procurements.



¹ <http://www.oracle.com/us/industries/communications/usm-volte-paper-2401569.pdf>

² <https://software.intel.com/en-us/articles/openstack-enhanced-platform-awareness>

³ <http://www.intel.com/content/www/us/en/architecture-and-technology/resource-director-technology.html>

⁴ <https://01.org/packet-processing/intel%C2%AE-quickassist-technology-drivers-and-patches>

⁵ <http://www.intel.com/content/www/us/en/architecture-and-technology/trusted-execution-technology/malware-reduction-general-technology.html>

⁶ <https://software.intel.com/en-us/articles/intel-advanced-encryption-standard-instructions-aes-ni>

⁷ <https://download.01.org/packet-processing>

⁸ www.openstack.org

⁹ <http://www.intel.com/content/www/us/en/communications/service-provider-network-maturity-paper.html>

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