Taylors Falls Reference Design for Intel® Xeon® D Processor in uCPE

intel.

Taylors Falls reference design, based on the Intel® Xeon® D processor, is an example hardware solution for Universal Customer Premise Equipment (uCPE). Taking advantage of the CPU's density optimizations in a power-efficient system-on-chip (SoC), the Taylors Falls reference design supports a breadth of converging edge workloads in a low cost, small footprint system.

Introduction

A foundation of the network transformation is the need to collect, manage, analyze, and store the explosion of data generated at network edges, combined with the enterprise adoption of cloud services. Communication service providers (CommSPs) and their ecosystem partners such as original design manufacturers (ODMs), independent software vendors (ISVs), telecommunications equipment manufacturers (TEMs), and system integrators (SIs) are now deploying customer premise equipment for network functions virtualization (NFV).

Universal CPE (uCPE) systems provide a single platform dedicated to a wide range of virtualized network functions including WAN routing, virtual private network, firewall, intrusion prevention system, session border control, carrier-grade network address translation, Wi-Fi, software-defined WAN (SD-WAN) and AI inference. A new approach to security, secure access service edge (SASE), for firewall, secure web gateway, cloud access service broker, and zero trust network access workloads is also supported. CommSPs are installing uCPE solutions to replace multiple fixed-function appliances, reducing potential capital and operating costs while providing increased service provisioning flexibility.

uCPE is compute, storage, and networking platforms to bring virtualized or non-virtualized services to small branch offices and small-to-medium-sized business. To support these platforms, Intel has developed the Taylors Falls reference design based on the Intel® Xeon® D-1700 processor. Built to deliver density- and power-optimized compute, the Intel Xeon D-1700 processor features advanced security and AI inference features, as well as per-core performance improvements over predecessors. The SoC package is highly integrated for simplicity and power efficiency, satisfying the requirements of small device form factors like uCPEs. Benefiting from the Intel® Xeon® D processor design, the compact, low-cost Taylors Falls solution provides TEMs, OEMs, and ODMs a product-ready design to bring uCPE servers to market very quickly.

This document is part of the Network Transformation Experience Kit, which is available at https://networkbuilders.intel.com/network-technologies/network-transformation-exp-kits.

Taylors Falls Reference Design

The Taylors Falls reference design based on Intel Xeon D-1700 processor highlights the CPU's balanced performance with low power and integrated features for uCPE solutions. For broad Communications Service Provider (CSP) use, it addresses network infrastructure uCPE solutions from customer premise to regional POP edges to data center edge. With this performant Intel® processor, an edge server based on the Taylors Falls architecture allows CSPs to quickly launch new revenue-generating services without adding new hardware in established deployments. Installation and future upgrades are simplified; truck rolls are reduced. Allowing small to medium businesses to virtualize equipment, new features can be easily downloaded, essentially growing "intelligence" in the same system.

The architecture supports the wide variety of connectivity interfaces required to accommodate the full range of uCPE applications and workloads.

Features in the Taylors Falls reference design include:

- Intel® Xeon® D-1700 processor optimized for density and delivered in power efficient SoC with built in hardware acceleration for cryptography, compression, and machine learning
- Compact design: 440 x 44 x 530 mm
- Built with lower cost off-the-shelf hardware
- Up to 384 GB DDR4 through 6x DDR4 RDIMM slots
- Multiple connectivity options: WWAN and WLAN, GNSS
- eMMC, M.2, SSD storage options
- BMC for system management
- Power over Ethernet – can supply power on 8 Ethernet ports
- Front panel with power modules, plugs, and all I/O for easy maintenance in cool zones including 8x 1GbE, 2x 25GbE and 2x USB3
- OCP 3.0 NIC
- 2x PCIe G4 / x8 expansion slots for accelerator cards
- 3x M.2 B-key slots for WiFi, 5G, or SSD support

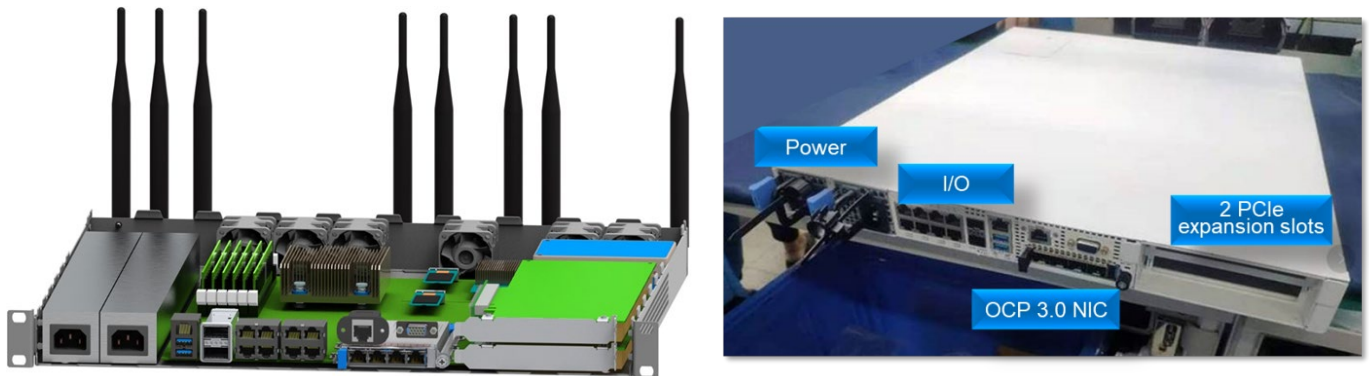Figure 1 depicts a 3D rendering of Taylors Falls, along with the finished system.

Figure 1. Taylors Falls system – 3D rendering (left) and Proof of Concept system

Schematics, board layout and documentation are provided in the reference design collateral.

Technologies Implemented

The Taylors Falls architecture takes full advantage of the broad range of interfaces and integrated functions of the Intel Xeon D processor SoC, including the following performance and security features:

- **Intel® Deep Learning Boost (Intel® DL Boost)** accelerates machine-learning workloads at the edge by eliminating unneeded precision in calculations so they can be completed more quickly.
- **Intel® AES New Instructions (Intel® AES-NI)** accelerates resource-intensive parts of the AES encryption algorithm in hardware.

- **Intel® Advanced Vector Extensions 512 (Intel® AVX-512)** boosts performance for demanding workloads with ultra-wide 512-bit vector operations that work on more data per clock cycle than predecessor platforms without Intel AVX-512.
- **Intel® QuickAssist Technology (Intel® QAT)** accelerates encryption and compression; the platform is capable of supporting up to 100 Gbps crypto and 70 Gbps compression functionality simultaneously.
- **Integrated Intel® Ethernet** provides up to 100 Gbps of throughput, with link options from 1GbE to 100GbE, low power consumption, and advanced storage support with Remote Direct Memory Access (RDMA).
- **Intel® Software Guard Extensions (Intel® SGX)** protects data while in use by creating private, isolated areas of memory called secure enclaves where unencrypted data can be operated on, beyond the reach of software and users, regardless of their privilege level.
- **Memory Encryption** supports existing software without modification while cryptographically protecting memory against hardware attacks using the NIST AES XTS encryption standard with hardware-generated keys from a hardened random-number generator implemented in silicon.
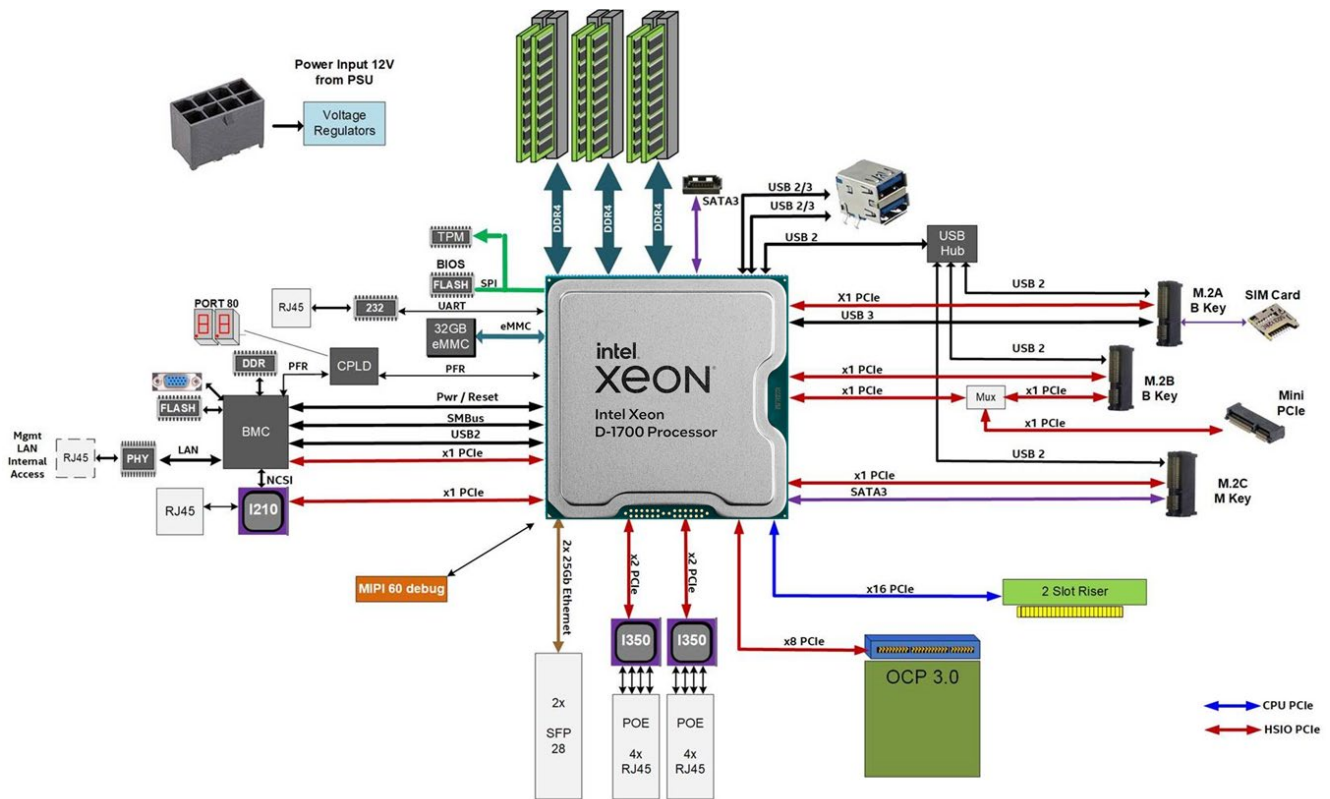

Figure 2. Taylors Falls architecture

The resulting design allows this single solution to address current and future virtualized network edge workloads on a single system.

Table 3. Features of Taylors Falls Systems

FEATURE	DESCRIPTION
CPU	Intel® Xeon® D-1700 processor, support 2 – 10c
Form Factor / Dimension	440 x 44 x 530 mm
Memory	6x DDR4 2400 – 29333MHz RDIMM Slots, 3 channels (SoC SKU dependent), max support 384GB
Network Support	2x 25Gbe integrated in CPU (support 25G and 10G) 8x 1GbE OCP 3.0 NIC

PSU	2x 850W AC/DC Power module, 1+1 Redundant, Hot swappable
Board Management	BMC Chip: ASPEED AST2500 BMC FW: Based on OpenBMC, IPMI 2.0, WebUI, Removes KVM
Other	2x USB3
Operating Environment	Temp: 0-35 C Humidity: 20%-90% RH
PCIe Expansion	2x x8 PCIe Gen4
Storage Capacity	1x 16GB eMMC 1x M.2 2280 SSD (SATA / PCIe x2) 1x 2.5" SATA SSD
Additional Connectivity Options	WWAN: 5G, LTE, 3G GNSS: GPS, Glonass, Galileo, BeiDou, QZSS WLAN: 802.11

Summary

uCPE based on Taylors Falls' flexible design with an Intel Xeon D Processor plays an important role the network transformation. Network service providers can converge multiple applications and services into the same server and readily deploy new ones as needed through remote software downloads. With the Taylors Falls reference design, a TEM, OEM, or ODM can begin a product today. The full reference design including schematics and layout files is available with a no cost license on the Intel Resource and Documentation Center.

Accton Technology* offers the SAF6101I Edge Server based on the Taylors Falls reference design. Visit Accton's website for more information.

References

Table 2.   References

TITLE	SOURCE
High Performance and Density with Low Power at the Enterprise Edge Solution Brief	https://networkbuilders.intel.com/solutionslibrary/high-performance-and-density-with-low-power-at-the-enterprise-edge-solution-brief
Enterprise Edge (uCPE): Introduction to uCPE and Edge Computing Course Chapter 1: Edge Computing: An Introduction	Intel® Network Builders Course https://networkbuilders.intel.com/university/course/enterprise-edge-ucpe-introduction-to-ucpe-and-edge-computing-1?vid=MTI4MA==
Intel Xeon D Processor Experience Kits	https://networkbuilders.intel.com/intel-technologies/intel-xeon-d-processor-experience-kits