

Encoding Video at the Edge with Intel® Xeon® Processors

Beamr 5* 4K HEVC encoder, adapted for the Intel® Xeon® processor E3 v5 product family with Intel® Iris® Pro graphics, enables real-time video encoding that responds rapidly to user-requested operations.

Beamr 5, a high-performance software HEVC video encoder, delivers broadcast-quality HDR and SDR video in real time. Using the Intel® Xeon® processor E3 v5 processor family, the encoder dramatically improves capabilities for just-in-time (JIT) transcoding to support emerging data-intensive formats.

- Encode 10-bit HDR 4Kp30 HEVC and 1080p60 video in real time
- Deliver responsive optimization for the wide range of playback devices in viewers' hands
- Retain the deployment flexibility of an all-software architecture

Executive Summary

As the video industry embraces future-focused technologies such as High Dynamic Range (HDR) and High Efficiency Video Coding (HEVC) while also supporting emerging applications such as 360-degree video and multi-camera programs, the need for more responsive encoding is on many people's minds. At the same time, second-screen devices are becoming more capable. With 4K Ultra-High Definition (UHD) now available on smartphones, the demand for advanced, device-optimized video is exploding—as is the complexity of video delivery.

A collaboration between Intel and Beamr, a video encoding and optimization company, offers the broadcast industry breakthrough options for software encoding content on low-power processors, increasing channel density to dramatically improve real-time operating performance and quality while reducing bitrate and storage requirements for service providers. The Beamr 5 4K HEVC encoder, running on the [Intel Xeon processor E3 v5 product family](#) with Intel Iris Pro graphics, makes JIT transcoding feasible at the network edge for today's high-value content and for future-facing content such as UHD with HDR, and 360 immersive video experiences, providing a competitive advantage in exceeding emerging customer expectations.

Emerging Use Cases

The need to deliver advanced video formats and low-latency applications to a wide range of devices is best addressed with architectures that execute JIT encoding at the network edge. Figure 1 illustrates one instance where this design is particularly relevant.

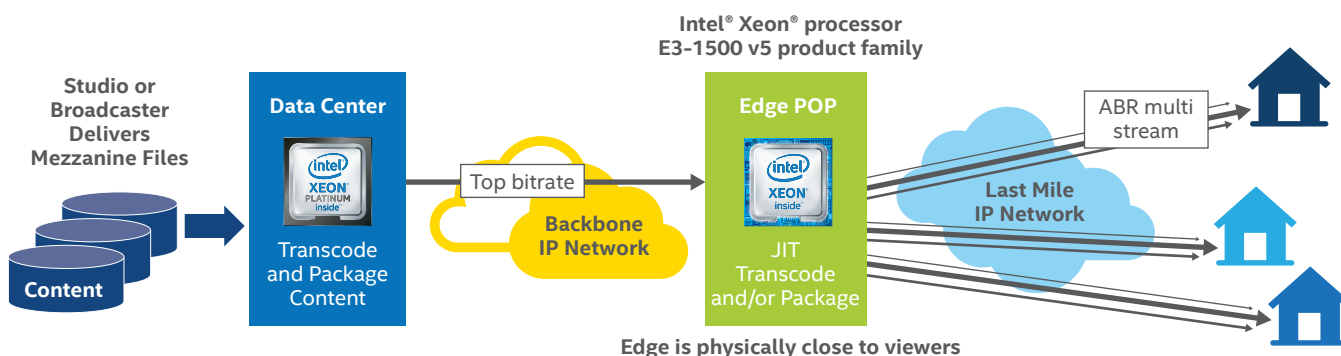


Figure 1. Edge-based processing for Over-the-Top (OTT) distribution.

In live broadcasts of sports, music, and political events, broadcasters may want to make multiple streams available simultaneously or supplement the traditional single feed managed by a director, enabling viewers to choose their own perspective on the event. In order to reduce last-mile bandwidth usage while meeting user expectations for high-quality experiences and low-latency requirements for real-time stream changes, final encoding is best performed near the viewer.

In a similar high-value use case, event broadcasts based on 360-degree immersive video streams deliver a complex, high bitrate stream, to be experienced as virtual reality on a normal TV display without the cumbersome goggles, as illustrated in Figure 2. Centralized cloud encoding systems cannot practically respond to such diverse viewing requirements. Broadcasters cannot afford to deliver the large streams necessary for quality viewing everywhere they're needed. Finally, last-mile networks and radio access networks that would try to accommodate such large streams risk congestion impacts on all their endpoints. However, delivering a single, high-quality feed to the edge enables a partitioned architecture. The edge processor can intercept user inputs, derive the requested view, encode it to meet the viewer device requirements, and deliver it in real time. The viewer benefits from a better experience, while the operator benefits from lower congestion and lower operating costs.



Figure 2. Segmented 360-degree immersive video would allow user to pan left or right.

For low demand, long-tail video on demand or for time-shifted cloud digital video recorder (DVR) content, edge encoding offers reduced delivery cost and increased security. The origin server needs to deliver only the top rate of the adaptive bitrate (ABR) ladder, and then the edge encoder creates the exact rendition required by the user's device. Thus, content owners need to create, store, and manage only a single rendition. At the edge, they can perform server-side ad insertion (also with a single rendition), bypassing ad blockers. They can also specify the various rate, geofencing,

and analytics policies, as well as local caching. For example, premium subscribers can be provided with higher quality feeds, while free viewers are offered only smaller feeds. Best of all, content providers can improve the viewer experience by dynamically managing the encoding parameters, relying on the innovative on-the-fly change capabilities of the Beamr 5 encoder to react to changing network congestion or to shape traffic to meet their service-level agreement commitments.

A New Generation of Encoding Capabilities

In April 2017, Beamr announced its real-time software-based video encoder capable of encoding live HEVC 10-bit HDR 4K video at 30 frames per second (fps) on the Intel® Xeon® processor E3-1585L v5.¹ This accomplishment empowers a range of edge computing applications running on low power, quad-core Intel® Xeon® processors. The encoder sets a new benchmark of performance and cost effectiveness when compared to predecessor platforms; as Beamr VP of Product Management Dr. Greg Mirsky points out, "In the past, it would have taken 16 to 24 cores, which were impractically large and power-hungry to deploy in edge-focused platforms."

The solution stack that integrates the Beamr 5 encoder, illustrated in Figure 3, offers significant total cost of ownership advantages for multiservice operators. The general-purpose nature of the Intel Xeon processor E3 family allows operators to offload selected workloads from central data centers, including functions such as content manipulation and management, as well as transcoding, packaging, digital rights management, ad insertion, and delivery. The commonality of software across Intel Xeon processors empowers operators to meet their needs with a mix of server architectures. The flexibility of deployment options maximizes the value that operators gain from their capital investments, as they consider alternatives to specialized hardware encoders. For example, the Intel Xeon processor's open architecture can be valuable for advanced video analysis utilized by the Beamr 5X content-adaptive encoder or for content management operations.

The Beamr 5 4K HEVC encoder offers customizable features for high performance, density, and video quality. It is an industry-leading, standards-compliant codec with support for 8-bit, 10-bit, and 12-bit color, and compatible with Dolby Vision*, HDR10, and Hybrid Log-Gamma (HLG). For second-screen and over-the-top (OTT) applications, Beamr 5 can deliver multiple output streams of different resolutions and bitrates from a single source and encoding instance, for efficient ABR delivery. Unique among encoders, it supports real time "on the fly" changes to operating parameters, enabling closed-loop control and management of network congestion.

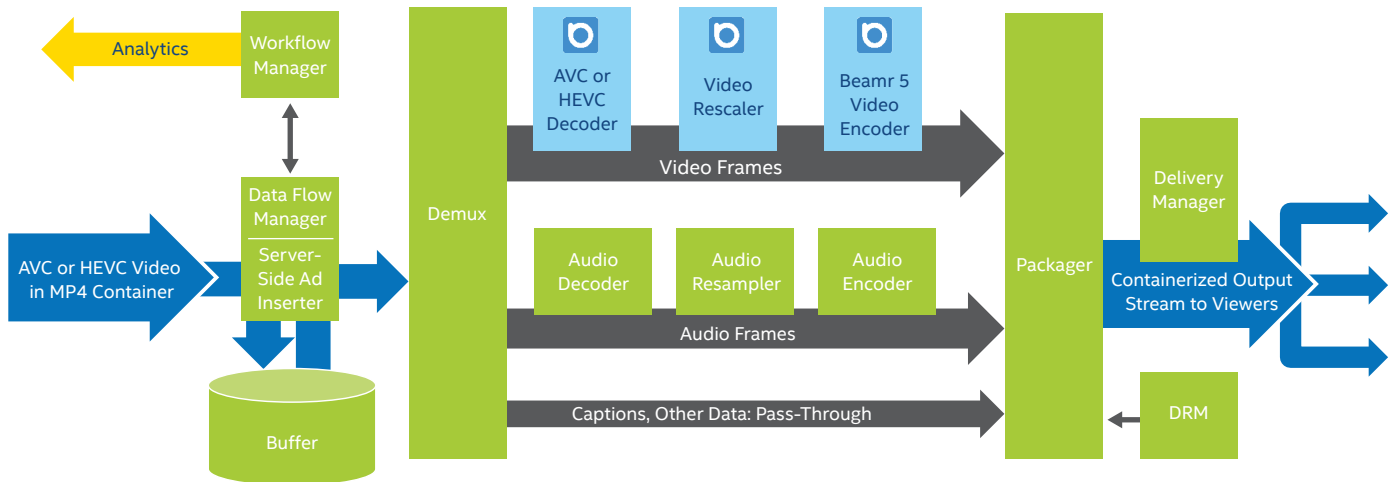


Figure 3. Beamr edge transcoder stack running on the Intel® Xeon® processor E3 v5 product family.

“The Beamr 5* 4K HEVC encoder running on the Intel® Xeon® processor E3 v5 product family with Intel® Iris® Pro graphics represents the highest density live software encoding solution in the market and is ideal for operators seeking capital cost and operational cost efficiencies.”

– Mark Donnigan, VP, Marketing, Beamr

The Beamr 5 4K HEVC encoder uses the integrated graphics of the Intel Xeon processor E3 v5 product family to encode H.265/HEVC, avoiding the extra cost, complexity, and power consumption of discrete graphics. Beamr 5 makes use of the following platform features:

- **Intel Iris Pro graphics P580** accelerates video transcoding with 72 execution units and 128 MB integrated on-package eDRAM memory, plus access to main system memory.
- **Updated OpenCL™ execution environment** reduces the need to re-establish recurring execution contexts and reduces context setup latencies dramatically.
- **Intel® Quick Sync Video** provides purpose-built dedicated, low-power, fixed-function video processing resources, integrated onto the processor die.
- **Intel® Advanced Vector Extensions 2 (Intel® AVX2)²** accelerates the vector-parallel computations required by video encoding algorithms.
- **High-speed memory support** by the Intel Xeon processor E3 v5 product family includes DDR4 RAM operating at 2133 MHz, for high data throughput.

Together, this combination of Beamr 5 software and the Intel® Xeon® processor E3-1585 v5 offer the following HEVC encoding capabilities (estimates are for 4:2:0 HDR 10-bit video; estimated throughput for SDR 8-bit content is expected to be 20 percent higher).

- **2160P (UHD):** One channel at up to 30 fps
- **1080P (HD):** Two channels at 60 fps or one channel at 1080p, then ABR of 720p, 480p, and 360p

Many system manufacturers offer motherboards, blades, and modules based on the Intel Xeon processor E3 product family that are designed to support the following operational configurations:

- **Appliances:** Single processor, standalone enclosures
- **Blades:** Chassis that accommodate from 4 to 18 blades, each hosting one or two processors, with various levels of PCI Express* and 10-Gigabit Ethernet communications between them
- **Modules:** Packaged in a high-density 4RU chassis capable of supporting up to 45 modules, each with one processor and high-throughput communication channels

Transcoding Considerations

The applications described so far, which reside at the edge of the network, accept input video at a relatively high bitrate and then transcode it for delivery to viewers. The transcoding application will need to integrate multiple components, among them a video decoder and encoder. The video encoder is the critical component in the system, and this brief focuses on the Beamr 5 HDR (10 bit) HEVC video encoder, which also encodes SDR (regular 8 bit) video at broadcast quality.

Two video decoder options are available:

- Intel Quick Sync Video hardware-assisted 8-bit (SDR) HEVC and AVC video decoders
- Beamr software decoders for 10-bit HDR HEVC or AVC video and 4:2:2 video

Conclusion

Video traffic already constitutes the largest portion of Internet traffic, and it is continuing to grow at greater than 70 percent CAGR. As multiservice operators migrate their infrastructure to become IP-based, as consumer devices with high-resolution screens and cameras proliferate, and as new content and applications emerge, providers will be faced with more kinds of content, more formats, and simply more content to deliver.

Beamr and Intel address this multidimensional challenge with a new architecture that simplifies key aspects of the problem, reduces the cost of delivery, and offers a better viewing experience. Although new to the video encoding world, the general architecture of origin and edge points of presence is already well established in content delivery networks. The high performance of the Beamr 5 encoder and the high density of Intel Xeon processor-based systems make it practical to employ this architecture to solve the needs of video encoding.

Find the solution that is right for your organization. Contact your Intel representative or visit intel.com/visualcloud.

Learn More

You may also find the following resources useful:

- [Beamr 5 4K HEVC Encoder Product Page](#) details the advantages, features, and benefits of the product and offers a free evaluation.
- [Intel® Xeon® Processor E3 Family Product Page](#) explores features, capabilities, and offerings for compute and visual workloads.
- [Intel® Network Builders](#) powers the visual cloud ecosystem by enabling hardware and software solutions for video delivery, cloud graphics, and media analytics.

Solution provided by:



¹ Intel® Xeon® processors E3-1585L v5 and E3-1578 v5 are also supported, albeit at different levels of throughput. Contact sales@beamr.com for details.

² Intel® Advanced Vector Extensions (Intel® AVX) provides higher throughput to certain processor operations. Due to varying processor power characteristics, utilizing AVX instructions may cause a) some parts to operate at less than the rated frequency and b) some parts with Intel® Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

Software and workloads used in performance tests may have been optimized for performance only on Intel® microprocessors. Performance tests, such as SYSmark® and MobileMark®, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <http://www.intel.com/performance/datacenter>.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No computer system can be absolutely secure. Check with your system manufacturer or retailer or learn more at www.intel.com.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Copyright © 2017 Intel Corporation. All rights reserved. Intel, the Intel logo, Iris, and Xeon are trademarks of Intel Corporation in the U.S. and other countries.

*Other names may be trademarks of their respective owners. 0917/EH/MESH/PDF 336314-001US

OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission by Khronos.