
intel
5G NEWORK TRANSFORMATION WITH FPGAS
PAT MEAD
INTEL NETWORK & CUSTOM LOGIC GROUP

DATA-CENTRIC INFRASTRUCTURE FOCUS

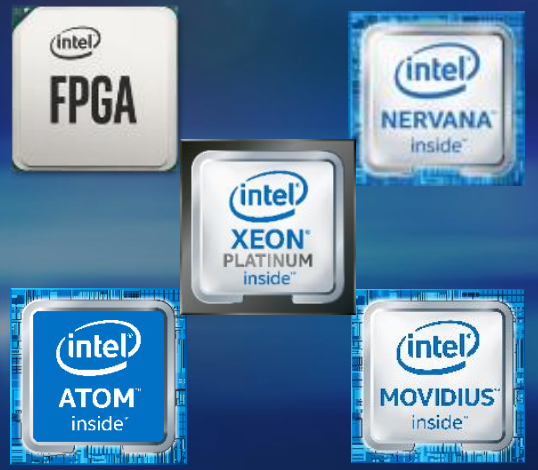
MOVE FASTER

- intel ETHERNET
- intel SILICON PHOTONICS
- intel OMNI-PATH FABRIC

STORE MORE

- intel OPTANE™ DC SOLID STATE DRIVE
- intel OPTANE™ DC PERSISTENT MEMORY

PROCESS EVERYTHING



SOFTWARE & SYSTEM-LEVEL OPTIMIZED

intel select solution

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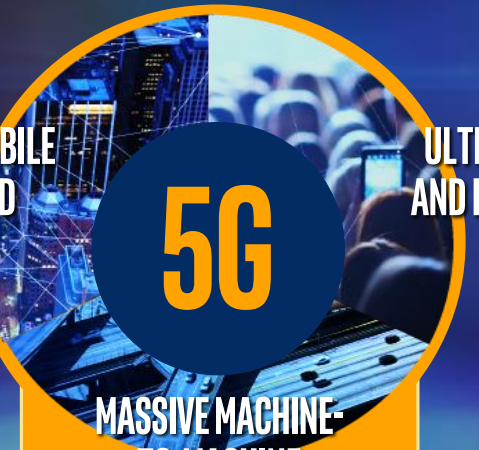
5G CONVERGENCE OF COMPUTE AND CONNECTIVITY

2G
CELLULAR COMMS

3G
DATA AND THE APP REVOLUTION

4G
FASTER DATA & MORE USERS



REQUIRES AGILITY, SCALABILITY AND INTELLIGENCE ACROSS NETWORK, CLOUD & CLIENT

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CLOUDIFICATION OF THE NETWORK

DATA CENTER | CLOUD | CORE | ACCESS | EDGE | DEVICES | THINGS

THE NETWORK MOVES TO INTEL® ARCHITECTURE (IA)

2011	2013	2015	2017	2019	2020
NFV DEFINED	**1ST NFV** PROOF OF CONCEPTS	**20%** OF COMMS SPS ADOPT NFV	**INTEL DPDK** MOVES TO LINUX FOUNDATION	**1ST 100%** CLOUD-NATIVE NETWORK	**75%** NETWORK WILL BE VIRTUALIZED

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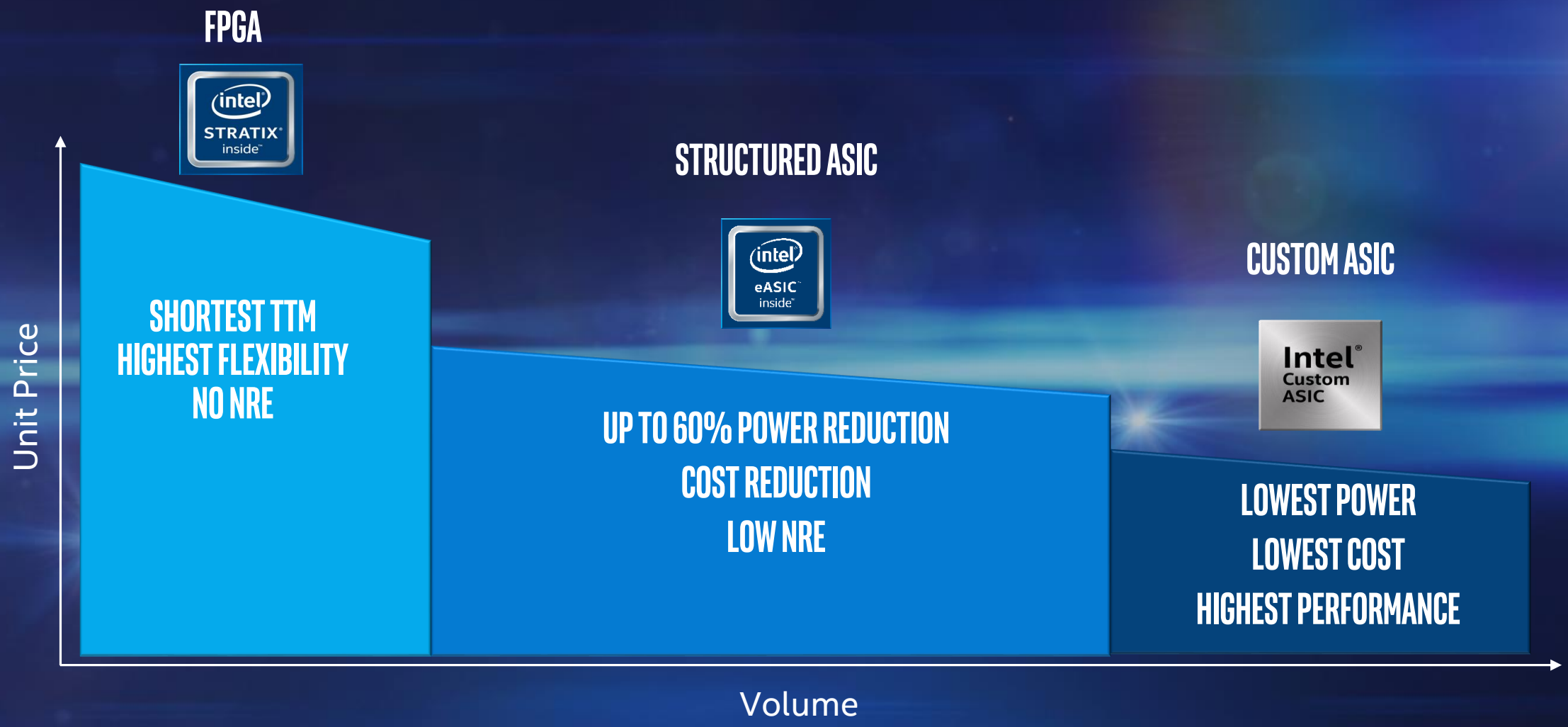
INTEL NCLG ENABLES E2E 5G

SCALABLE & FLEXIBLE TECHNOLOGIES AND OPEN SOURCE

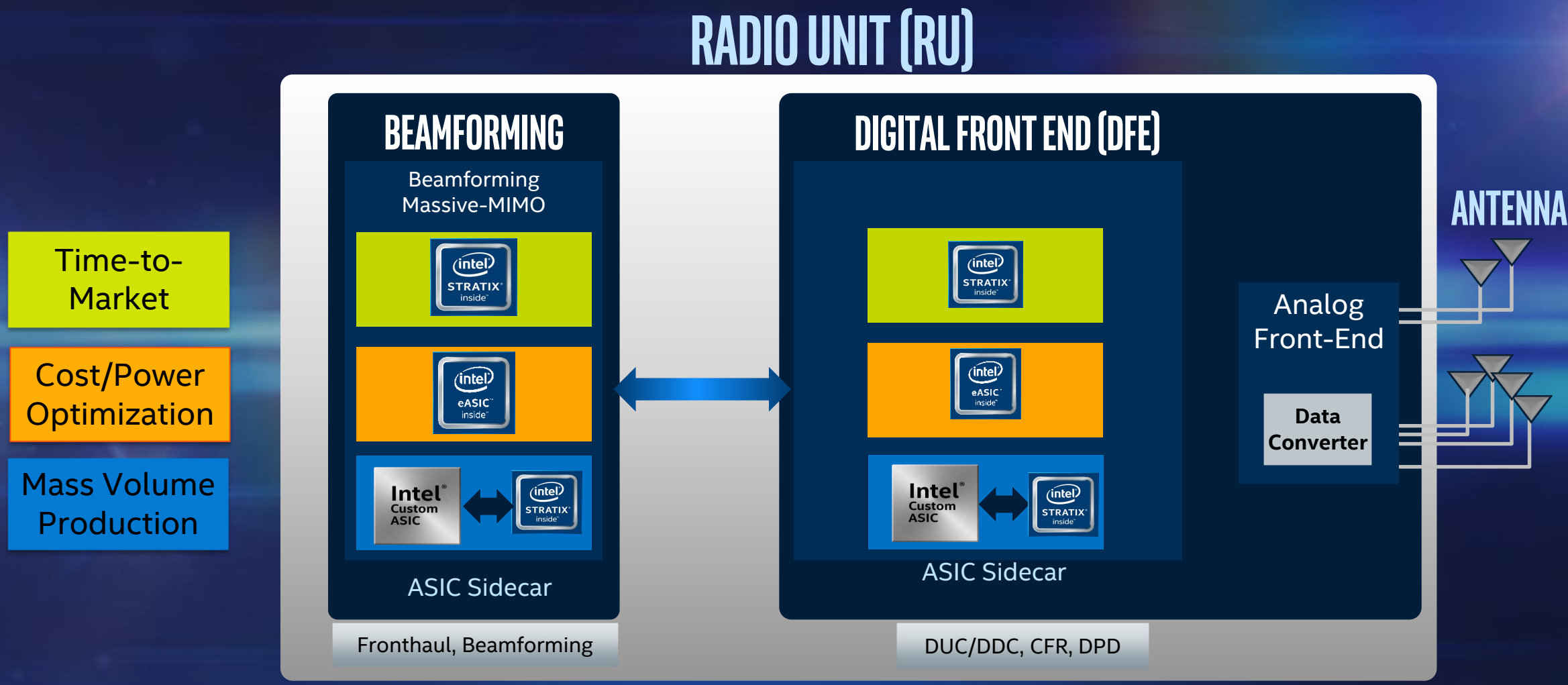
Radio	FlexRAN	5GCN / vEPC
Front Haul	MEC	NFVI
Baseband	Back Haul	Security

THE COMPLETE CUSTOM LOGIC PORTFOLIO



MOVE TO THE LOWEST COST, LOWEST POWER SOLUTION AS VOLUMES GROW AND STANDARDS MATURE

5G RADIO SOLUTIONS



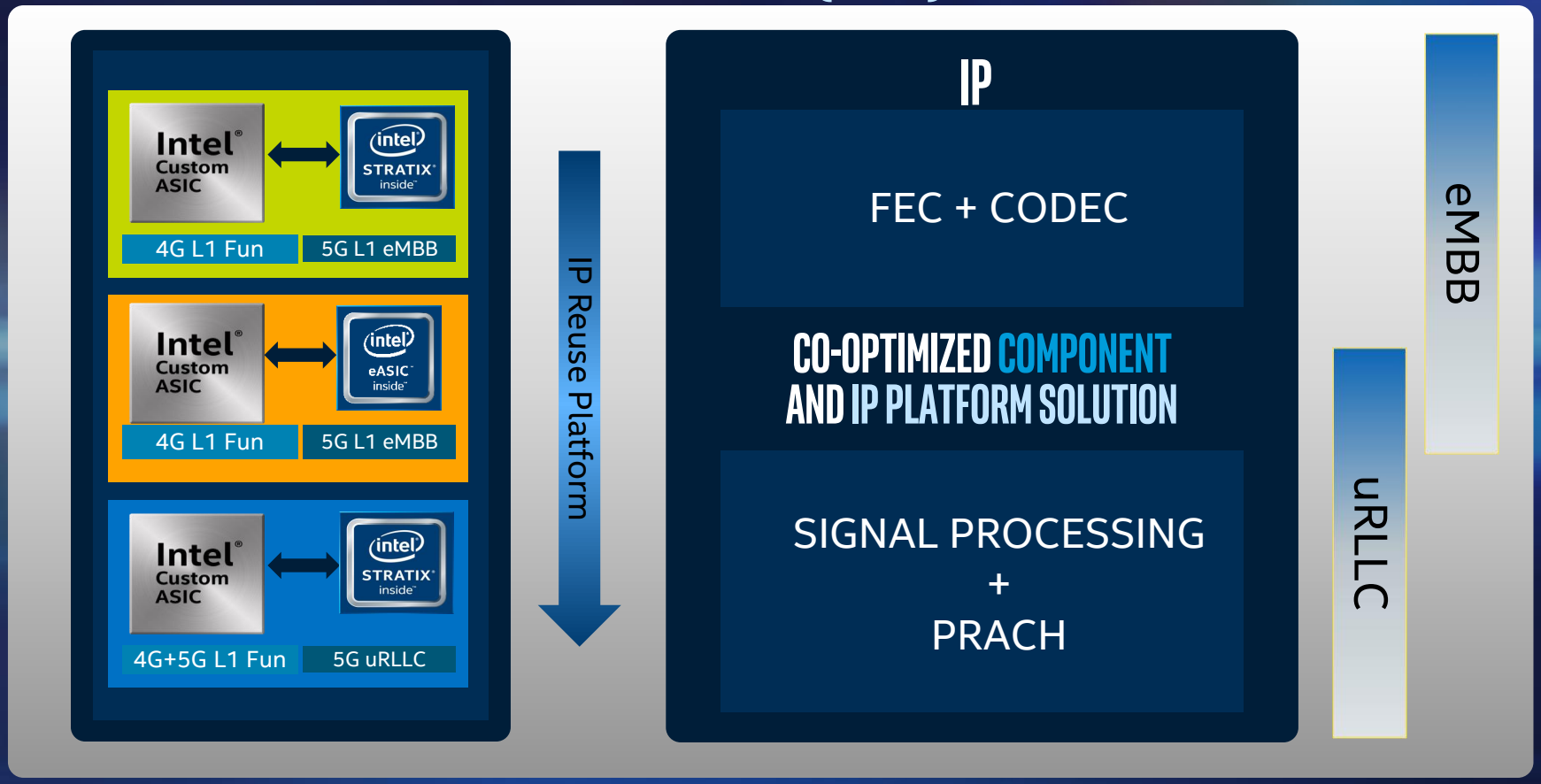
5G BASEBAND SOLUTIONS

BASEBAND UNIT (BBU)

Time-to-Market

Cost/Power Optimization

Mass Volume Production



FLEXIBLE FRONTHAUL SOLUTIONS

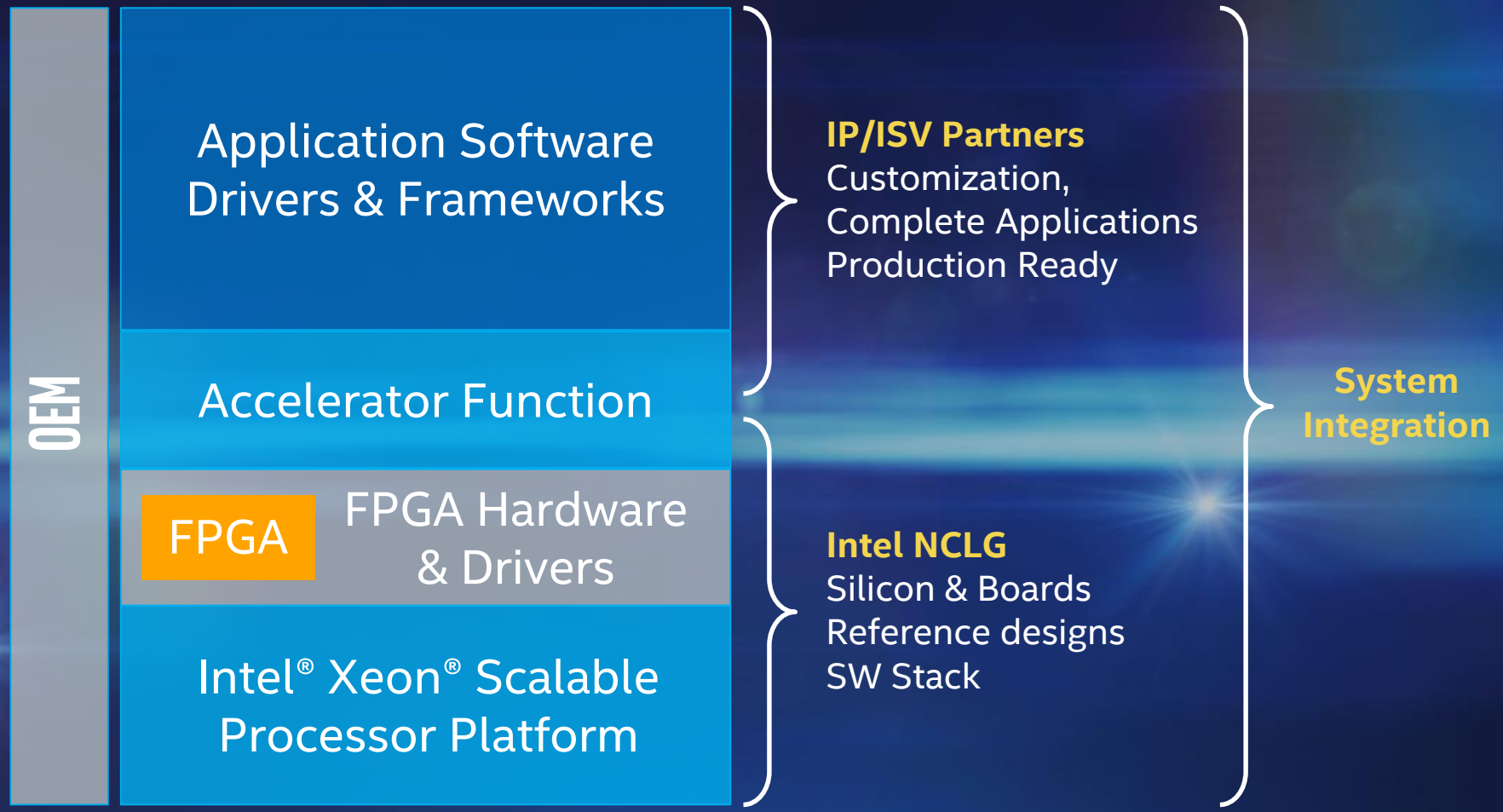
FRONTHAUL SOLUTIONS SUPPORTED ACROSS XEON, FPGA & EASIC DEVICES

CONNECTIVITY and FLEXIBILITY

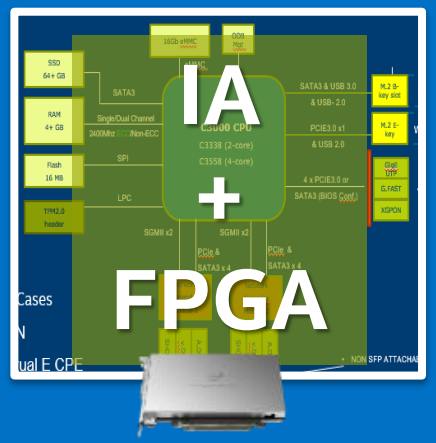
TECHNICAL STANDARD REFERENCE DESIGN AND LEADERSHIP

- CPRI IP
- eCPRI IP
- RoE IP
- Compression IP
- xRAN IP
- Synchronization & 1588 IP

SOLUTION COMPONENTS & ECOSYSTEM



ECOSYSTEM ENABLEMENT MODEL FOR VRAN



COTS Architecture, Server Platforms (Intel® Xeon® D processor, Intel® Xeon® Scalable Processor), FPGA PAC

Intel FlexRAN & vRAN Enablement Package

L1 (PHY) 4G & 5G

L2 / L3 (Stack) 4G & 5G

3rd Party SW

RRU

OEM/TEM/SI vRAN Solution (BBU on COTS Server & SW, FPGA, RF and RRU)

BBU SW

4G & 5G vRAN Solutions

Service Providers

Enterprises

Platforms

Reference S/W & User Workload Optimized on IA/FPGA

Commercial Product

Intel working with eco-system to accelerate the development of vRAN solutions

INTEL RAN SOLUTION PORTFOLIO

Intel® Xeon® Processor

Intel Atom® Processor

Artificial Intelligence

Intel® FPGA

Intel® eASIC

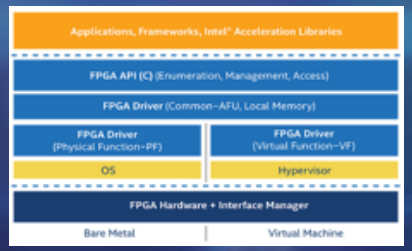
ASIC

Application Specific Products

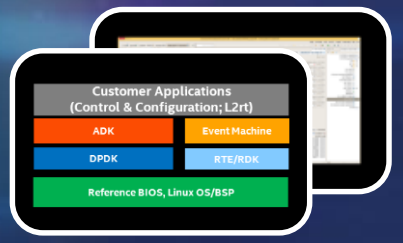
Custom Modules

Intel® PAC

Enablement Software



Open Programmable Acceleration Engine (OPAE)



Wireless Transport Production SW

Intel® FlexRAN Reference SW

Standards & Industry Consortia

3GPP A GLOBAL INITIATIVE

IEEE

ETSI

xRAN

TELECOM INFRA PROJECT

O-RAN ALLIANCE

Intel brings together the products, ecosystem & influence to enable next generation RAN architectures

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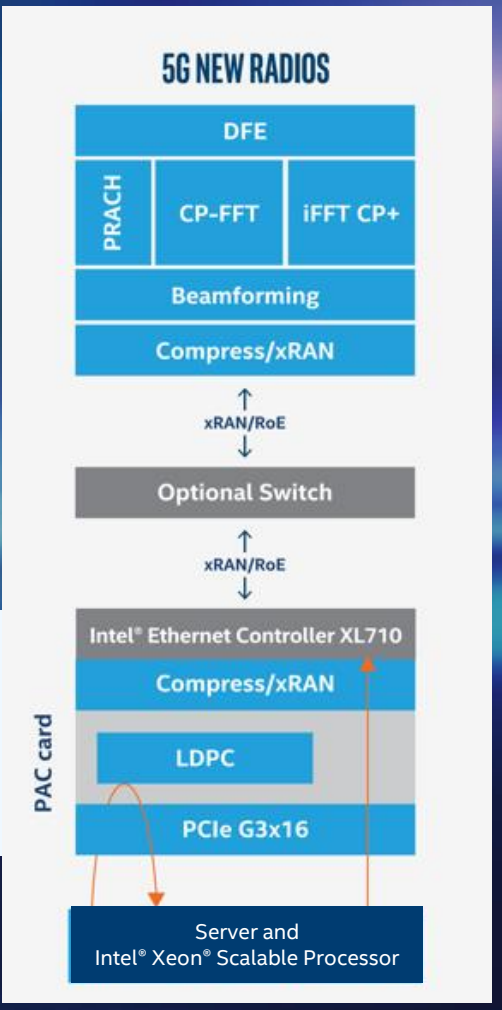
INTEL® PAC N3000 – 4G & 5G L1 ACCELERATION

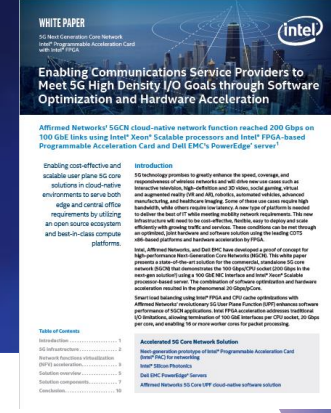
Intel® PAC N3000 Acceleration Card

- Integrated Reference Design for **LTE Turbo (FEC)**, **5G LDPC (FEC)** and **XRAN/ORAN Fronthaul**
- **Flexibility of repurposing** same hardware for different workloads
- DPDK API (BBDev) for FlexRAN PHY integration, OPAE Tools
- PCIe Gen3 x16, 2xQSFP28, Full Height, Half Length

Reference Design Program for OEM development and ecosystem partners

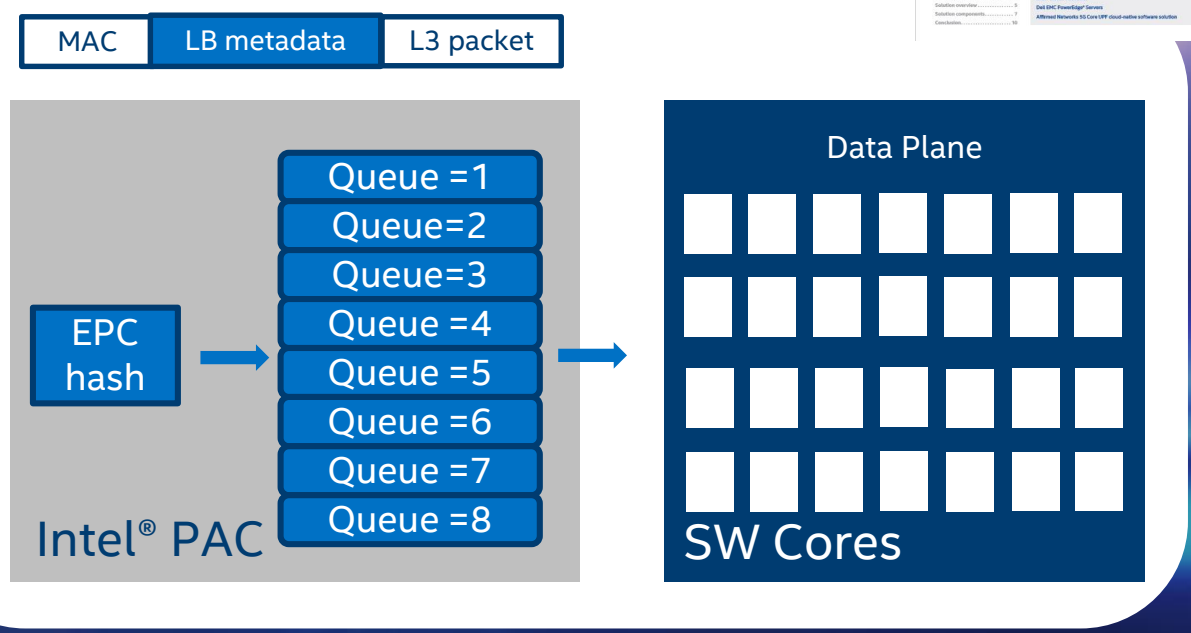


LOAD BALANCING ACCELERATOR



Overview

- Achieved 170 Gbps on 2 x 100 GbE links using Intel® Xeon® processors and Intel® FPGA-based Programmable Acceleration Card*
- Enabling cost-effective and scalable user plane 5G/4G core solutions for both edge and central office requirements by utilizing COTS platforms



Value

- Packet processing performance improvement with optimized CPU utilization
- Frees up cores for other hosted 5G services, e.g. DPI
- Reduced CapEx/OpEx

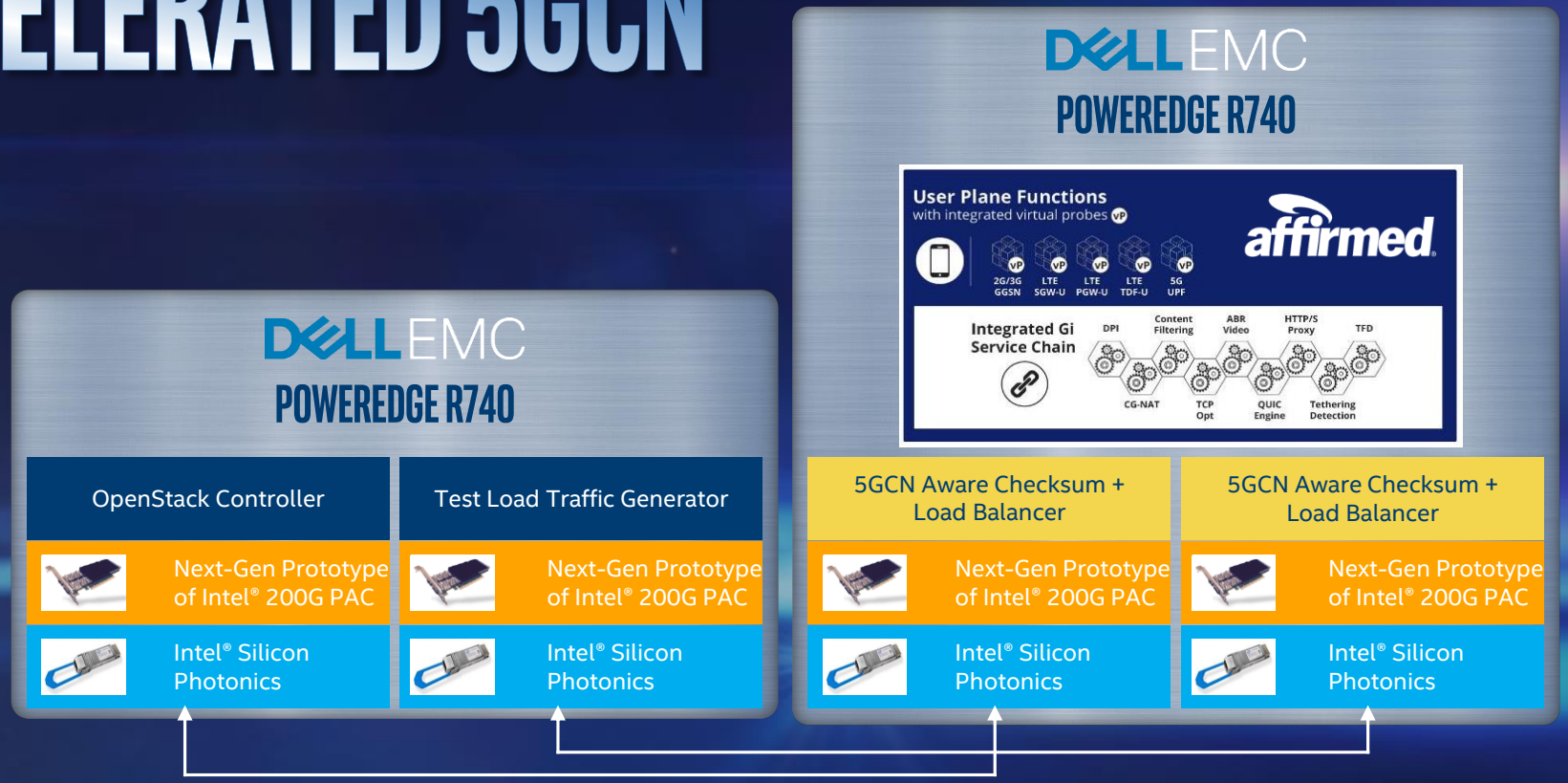
Performance Gain

- 50% core saving on user plane forwarding
- 100 GbE termination
- 20 Gbps / core

* Source : Affirmed Networks Benchmarks – Configuration on next slide

200G FPGA-ACCELERATED 5GCN

- First cloud-native containerized 5G core network with 100GbE interfaces (MWC 2019)
- Load balancing acceleration using Intel® PAC
- Affirmed 5GCN SA VNF
  - User plane packet forwarding
- HW accelerated load balancing free up 12 physical core available for DPI and/or other applications



#pCPU User	Traffic Type: 50/50 Uplink/Downlink	Throughput per Server	Packet Rate per Server	Details*
12	UDP, 640 Bytes Packet	~170 Gbps	33 Mpps	• Intel® Skylake Platinum with 200 Gbps line rate • Demo and corresponding core were based on 5GCN packet forwarding • Application headroom with 44 pCPUs out of 56 pCPUs in 2 socket server with 170 Gbps throughput at application level and 193 Gbps line rate.
8	UDP, 640 Bytes Packet	~160 Gbps (20 Gbps/pCore)	31 Mpps	

* Source : Affirmed Networks Benchmarks

COMMUNICATIONS FPGA ECOSYSTEM

ALTIOSTAR	*Leading solutions provider for End-to-End 4G & 5G wireless*
affirmed	*Leader in accelerated vEPC and 5GCN solutions*
f5	*Leader in Firewall and Network Management*
Arrive	*Leader in accelerated IPSec and TLS security IP*
benu NETWORKS	*Leader in accelerated vBNG and vCPE solutions*
HCL	*Global Design services and System Integration partner*

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THANK YOU